REMARKS

With this response, claims 12, 19 and 39 are amended. No claims are added. Claims 44 and 46-49 are canceled. Therefore, claims 1-4, 7, 10-15, 19, 39 and 40 are pending.

REJECTIONS UNDER 35 U.S.C. § 112

Claims 1-4, 7, 10-15, 19, and 39-40 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the invention.

Claims 12 and 19 were rejected for failing to provide an antecedent basis for the term "the buffer level." Applicants have amended these claims to recite the limitation "a buffer level," and therefore respectfully request the withdrawal of this rejection.

Claims 1, 14 and 39 were rejected because the Office Action asserts that it is unclear what is the relation between the limitations "monitoring the state of the multi-threaded application" and "[monitoring] the buffer," and that it is unclear what is meant by "state of multi-threaded application." Applicants contend that a "state of application" clearly describes what the application may be doing at an observed time. For example, Applicants respectfully point out that paragraph [0026] of the Specification discloses that an application state may indicate said application is "streaming data" to a buffer. Furthermore, said buffer may have a state related to use (e.g., occupied) or a state related to fullness (e.g., underflow, overflow). Thus, in view of the examples from the Specification discussed above, "monitoring the state of the multi-threaded application" may result in observing that an application is streaming data to a buffer, and "[monitoring] the buffer" may result in observing how full the buffer is. Thus, Applicants contend that the above limitations are clear and distinct on their face, and that they are clear and distinct in light of the teachings of the Specification. Therefore, Applicants respectfully request the withdrawal of this rejection.

The Office Action further asserts that it is unclear how the coordination of the thread dispatch increases execution overlap. Applicants contend that these claim limitations are clear, that threads may be dispatched in a manner to increase execution overlap. Applicants respectfully point out that FIG. 4A illustrates an example of dispatching threads of a multi-threaded application to increase execution overlap. Applicants contend that these limitations

satisfy the requirements of 35 U.S.C. § 112 second paragraph and respectfully request the withdrawal of this rejection.

Claim 39 was further rejected as the Office Action asserts that the limitations "the buffer" and "the system buffer" are appear in the claim, yet appear to refer to the same thing. Applicants have amended this claim to consistently recite "the system buffer" and thus respectfully request the withdrawal of this rejection.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 11-14, 19, and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0115428 of Zaccarin et al. (hereinafter "Zaccarin"), in view of U.S. Patent Application Publication No. 2001/0056456 of Cota-Robles (hereinafter "Cota-Robles").

Applicants respectfully contend that these claims are not rendered obvious by the cited references for at least the following reasons.

I. The references, alone and in combination, fail to disclose or suggest at least one feature of the invention as recited in the independent claims.

Claim 1 recites dynamically adjusting one or more of a frequency or the voltage applied to the processor **based, at least in part**, on the availability of the buffer and **the coordination of the dispatch of the threads** of a multi-threaded application. Independent claims 14 and 39 recite similar features.

The Office Action on page 4 cites paragraphs [0015]-[0017] of Zaccarin to disclose the above feature of the independent claims. Applicants respectfully disagree.

Paragraph [0015] of Zaccarin discloses "the level of the data **buffer** 14 indirectly controls the frequency and voltage of the processor by increasing voltage & frequency when the buffer level is high, and reducing voltage and frequency when the buffer level is low." No other disclosures in paragraphs [0015]-[0017] of Zaccarin are directed towards adjusting processor frequency or voltage. Thus, even assuming for the sake of argument that Zaccarin may be cited to disclose adjusting processor frequency or voltage based on a buffer level, Zaccarin **fails** to disclose further adjusting the processor frequency or voltage based on the dispatch of threads of a multi-threaded application. In contrast, independent claims 1, 14 and 39 recite dynamically adjusting one or more of a frequency or the voltage applied to the processor **based, at least in**

part, on the availability of the buffer and **the coordination of the dispatch of the threads** of a multi-threaded application. Therefore, Applicants contend that Zaccarin fails to disclose the above features of the independent claims.

Cota-Robles fails to cure the defects of Zaccarin as Cota-Robles contains no disclosures directed towards adjusting processor frequency or voltage based on the dispatch of threads of a multi-threaded application. Therefore, no combination of Zaccarin and Cota-Robles discloses the above feature of the independent claims.

II. The Office Action fails to make clear the reasoning as to why "changing frequency/voltage of a processor based on availability of the buffer" is equivalent to "coordinating the dispatch of threads by changing the dispatch rate based on availability of the buffer."

The Office Action on page 5, paragraph 11, admits that the combination of Zaccarin and Cota-Robles ***fails*** to disclose "determine the availability of the processor" and "coordination of dispatch of threads based at least in part on availability of the buffer," but that both would be obvious to one of skill in the art.

With regards to the limitation "determine the availability of the processor" as described by the Office Action, Applicants contend that said quotation of the independent claims is incomplete with respect to the actual recitations of the independent claims, as the independent claims clearly recite "determining availability of a processor to perform simultaneous multi-threading." Applicants respectfully point out that "**[a]ll words in a claim must be considered** in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970) (as cited by MPEP § 2143.03). Applicants further point out that

> [R]ejections on obviousness **cannot be sustained with mere conclusory statements**; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). See also *KSR,* 550 U.S. at 398 (2007) (quoting Federal Circuit statement with approval, and further holding that the analysis for supporting a rejection under 35 U.S.C. § 103 should be made ***explicit***).

The Office Action has not considered all words of the independent claims, and further fails to articulate a rational, explicit line of reasoning as to why the above limitation is obvious. Therefore, Applicants contend that the Office Action's rejection of the limitation "determining availability of a processor to perform simultaneous multi-threading" is improper.

With regards to the limitation "coordinating the dispatch of threads of the multi-threaded application based at least in part on the availability of the buffer" as described by the Office Action, Applicants further contend that the said quotation of the independent claims is incomplete with respect to the actual recitations of the independent claims, as the independent claims clearly recite "coordinating dispatch of threads of the multi-threaded application to ***increase execution overlap of activities executing*** in the system based, at least in part, on the availability of the buffer." The Office Action again has not considered all words of the independent claims, and further fails to articulate a rational, explicit line of reasoning as to why the above limitation is obvious. Therefore, Applicants contend that the Office Action's rejection of the limitation "coordinating the dispatch of threads of the multi-threaded application based at least in part on the availability of the buffer" is improper.

Applicants contend that the rejections of independent claims 1, 14 and 39 are deficient for at least the reasons discussed above. Claims 11-13 and 19 each depend from one of the independent claims discussed above. Per MPEP § 2143.03, claims that depend from nonobvious independent claims are likewise nonobvious over the references.

Claims 2-4, 15, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles, and further in view of U.S. Patent No. 6,662,203 of Kling et al., (hereinafter "Kling"). The deficiencies of Zaccarin and Cota-Robles with respect to independent claims 1, 14 and 39 are discussed above. Kling fails to cure the above deficiencies of Zaccarin and Cota-Robles, as Kling contains no disclosures directed towards the limitations of the independent claims discussed above. Therefore, no combination of Zaccarin, Cota-Robles and Kling may be cited to disclose the independent claims. Each of claims 2-4, 15 and 40 depend from one of the independent claims discussed above. Per MPEP § 2143.03, claims that depend from nonobvious independent claims are likewise nonobvious over the references.

Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles as applied to claim 1 above, and further in view of U.S. Patent No. 4,811,208 of Myers et al., (hereinafter "Myers"). The deficiencies of Zaccarin and Cota-Robles with respect to independent claim 1 are discussed above. Myers fails to cure the above deficiencies of Zaccarin and Cota-Robles, as Myers contains no disclosures directed towards the limitations of independent claim 1 discussed above. Therefore, no combination of Zaccarin, Cota-Robles and Myers may be cited to disclose independent claim 1. Claim 10 depends from

independent claim 1. Per MPEP § 2143.03, claims that depend from nonobvious independent claims are likewise nonobvious over the references.

Claim 10 was also rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles and Myers, as applied to claim 7 above, and further in view of U.S. Patent Application Publication No. 2002/0188884 of Jain et al (hereinafter "Jain"). The deficiencies of Zaccarin, Cota-Robles and Myers with respect to independent claim 1 are discussed above. Jain fails to cure the above deficiencies of Zaccarin, Cota-Robles and Myers, as Jain contains no disclosures directed towards the limitations of independent claim 1 discussed above. Therefore, no combination of Zaccarin, Cota-Robles, Myers and Jain may be cited to disclose independent claim 1. Claim 10 depends from independent claim 1. Per MPEP § 2143.03, claims that depend from nonobvious independent claims are likewise nonobvious over the references.

CONCLUSION

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, all pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
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I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

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